Lab 4. CARRIER SYNCHRONISATION

Total marks: 5 marks

1. Lab introductions

Carrier synchronisation refers to the requirement for coherent digital receivers to recover an in-phase version of the carrier at the receiver. There are two general cases here: carrier recovery when a pilot tone is present; and carrier recovery without a pilot tone.

We will study the technique of carrier synchronisation using phase-locked loop (PLL). Its purpose is to track the carrier frequency of the input signal to allow the coherent demodulator to remove the carrier from the received bandpass signal and map it to baseband. Although receiver generally knows the value of carrier frequency in transmitter side, many factors may still result in a frequency difference between received signal carrier and local carrier. One major factor is Doppler shift, which is caused by the moving of transmitter/receiver or reflectors. Also, it might be introduced by the frequency drift of an oscillator from its nominal frequency. Causes may include component aging, changes in temperature that alter the piezoelectric effect in a crystal oscillator, or problems with a voltage regulator which controls the bias voltage to the oscillator.

In this lab, we will focus on the basic form of PLL as shown in Fig.1, which consists of a variable frequency oscillator (VCO) and a phase detector (Multiplier + Lowpass Filter) in a feedback loop.

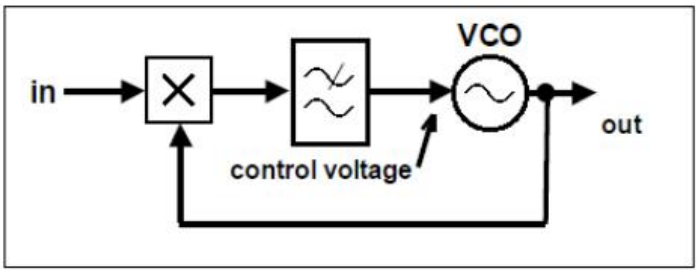


Fig. 1 The basic PLL

This lab consists of two experiments, namely Experiment 1 –Properties of PLL, and Experiment 2 – PLL assisted BPSK coherent demodulation. In Experiment 1, pure sine wave is used as the input to measure the lock range of PLL. In Experiment 2, we will study the demodulation performance of BPSK + Pilot Tone, with a PLL in receiver end to obtain the carrier.

Both experiments are carried out in the platform of **Matlab-Simulink**. You can access Matlab 2019b in UNSW myAccess without installing the software in your own computer. For instructions, please see Appendix A.

Simulation source files, i.e., Lab4a.SLX, Lab4b.SLX**,** and video demonstration are provided to assist you in this lab. What you need to do with the provided source files is to change the

parameters as per Quiz Questions, and observe the output. **A report that addresses Quiz Questions is expected as the output of this lab, and based on which a mark will be given as part of the assessment of this course.**

(a) Experiment 1. Properties of PLL

Open the file Lab4a.SLX in MATLAB 2019b, which is available in the link below.

https://weiwang-wys.github.io/files/Lab4/Lab4a.slx

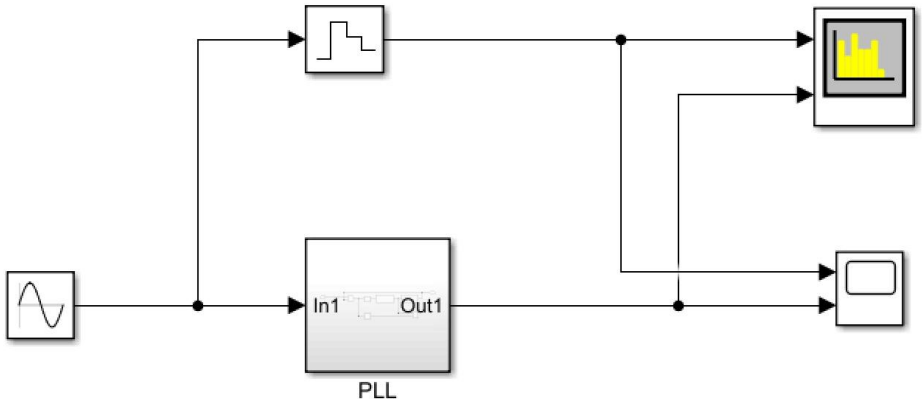


Fig. 2 (a) Block diagram of Experiment 1 (Lab4a.SLX)

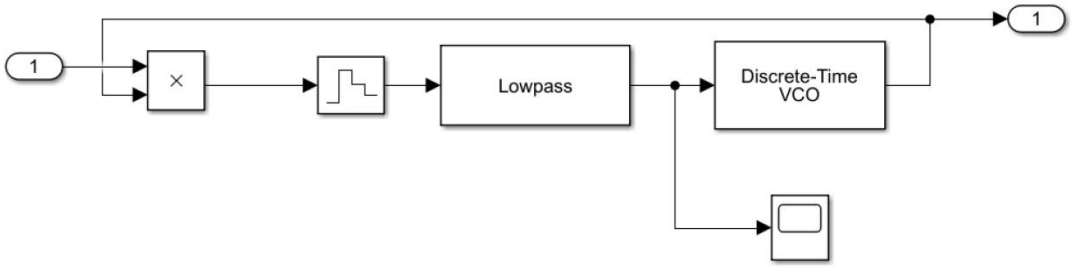


Fig. 2(b) Structure of the subsystem PLL

In Fig. 2(a), sine wave is used as the input of basis PLL, and the structure of PLL is shown in Fig. 2(b). The quiescent (center) frequency of VCO is 8kHz and frequency of the input sine wave is 8kHz +Δf. Descriptions of each module in Fig. 2 are given in Appendix B. In this experiment, you are required only to change frequency of the input sine wave and record the 'pull-in' range of PLL. To measure 'pull-in' range, please gradually increase/decrease the frequency of sine wave to find the transition point from **'unlock'** to **'lock'**.

'Lock' --- In the state of lock, the frequencies of the output and input of PLL are identical, and there exists a constant phase difference between output carrier and input carrier. Thus, we say

that the phase difference between input signal and output signal is locked.

'Unlock' --- In the state of unlock, frequencies of the output and input of PLL are different, and the phase difference between output carrier and input carrier is thus time-variant due to the frequency gap. Therefore, we say that the phase difference between input signal and output signal is unlocked.

For detailed instruction, please watch the following video.

https://weiwang-wys.github.io/files/Lab4/Lab4a.mp4

Quiz Question 1. Please measure the pull-in range of the given PLL with VCO gains 100Hz/V, 200Hz/V and 400Hz/V, respectively. Examine whether this 'pull-in' range is dependent on the VCO gain, and if so, how it is dependent?

VCO gain (Input sensitivity)	**'Pull-in' Range***
100 Hz/V	
200Hz/V	
400Hz/V	

***'Pull-in' range is in the form of [8kHz-f_1, 8kHz+f_2]

(b) Experiment 2. PLL assisted BPSK coherent demodulation

Open the file Lab4b.SLX in MATLAB 2019b, which is available in the link below.

https://weiwang-wys.github.io/files/Lab4/Lab4b.slx

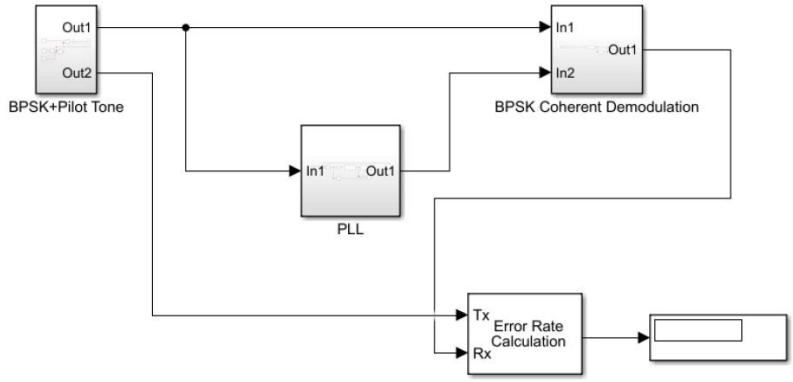


Fig. 3 (a) Block diagram of Experiment 2 (Lab4b.SLX)

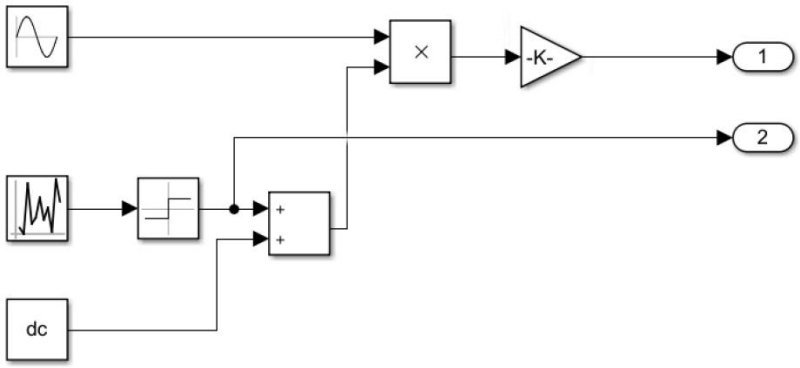


Fig. 3(b) Structure of the subsystem BPSK + Pilot Tone

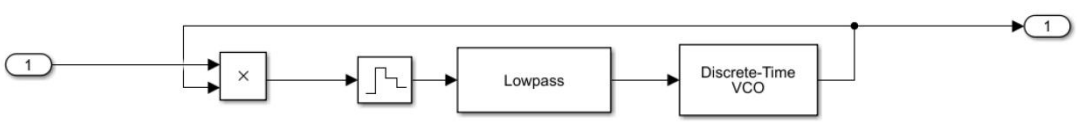


Fig. 3(c) Structure of the subsystem PLL

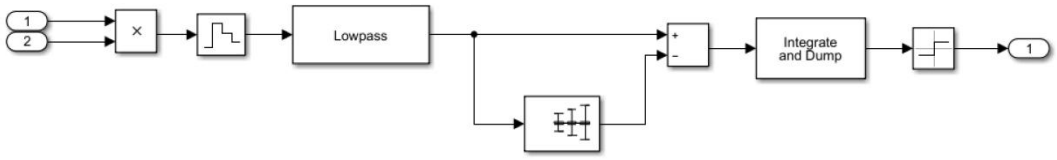


Fig. 3(d) Structure of the subsystem BPSK coherent demodulation

This experiment studies the performance of coherent demodulation of BPSK + pilot tone with a PLL in receiver to acquire the carrier. Note that quiescent (center) frequency of VCO is 8kHz and carrier frequency of BPSK + Pilot Tone is 8.02kHz, which means that PLL needs to track the carrier frequency and compensate for the 20Hz frequency shift.

Descriptions of each module in Fig. 3 are given in Appendix B. For detailed instruction, please watch the following video.

https://weiwang-wys.github.io/files/Lab4/lab4b.mp4

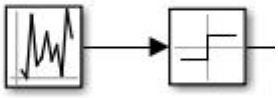
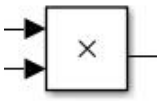
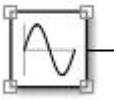
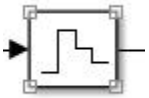
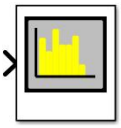
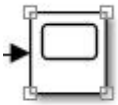
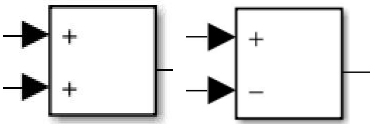
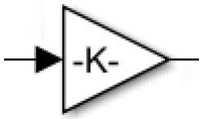
Quiz Question 2. What fraction of signal power is used to transmit the pilot tone when dc = 0v, 0.5v, 1v, 1.5v, 2v, respectively? Then, please record the corresponding BER. How does BER change with pilot tone power ratio?

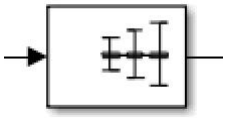
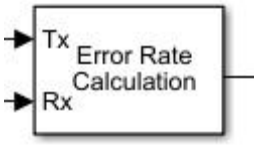
DC voltage*	Power Ratio of Pilot Tone#	BER
dc=0v		
dc=0.5v		
dc=1.0v		
dc=1.5v		
dc=2.0v		

*** To set the value of dc, please type command in Command Window of Matlab**

 # Amplitude of binary sequence is 1v in the sub-system --- BPSK + Pilot Tone

Appendix A-- Description of modules

	Binary sequence generator which generates random binary sequence with the values being -1 and 1.
	Multiplier
	Sine wave generator
	Zero-order hold, which works as a sampler (a.k.a ADC, analog-to-digital converter)
	Spectrum Analyzer
	Scope
	Adder/Subtractor
	Gain, which multiple its input with a multiplicative coefficient. This module is used to normalize the power of BPSK + Pilot Tone
	Lowpass Filter

	Mean, which computes the mean value along the specified dimension of the input or across time (running mean). This module, together with the subtractor, is used to remove the DC component of lowpass filter output.
	Integrate and Dump: Integrate over the number of samples in the integration period and reset at the end of the integration. The integrate-and-dump circuit is a *correlator* whose output equals the matched filter output **only at the sampling instants**, and not in-between.
	Error Rate Calculator, which computes the error rate of the received data by comparing it to a delayed version of the transmitted data.